Amendments to Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A processor comprising:

instructions with at least one operand field, the instructions comprises immediate instructions having immediate data in the operand field;

a data table for storing immediate data, wherein immediate data are stored in the data table in an order determined by a flow analysis, the data table enables immediate data to be separated from the instruction stream;

a program counter for storing an instruction address of an instruction, wherein the processor fetches an instruction from the instruction address in the program counter during program execution; ~~and~~

an instruction decoder for decoding the instruction fetched by the processor, wherein ~~an~~ immediate data from the data table is provided to the processor if the instruction fetched is an immediate instruction;

an instruction register coupled to the instruction decoder, the instruction register stores the instruction fetched by the processor during program execution and passes the instruction to the instruction decoder for decoding; and

a data table addressing unit coupled to the data table and the instruction register, the instruction register passing relative addressing information contained in the instruction to the data table addressing unit when the decoder decodes the immediate instruction, the relative addressing information, which comprises an index and a format indicator, is used to provide an address of the immediate data in the data table,

wherein the data addressing unit comprises a data table pointer containing a value,

if the format indicator comprises a post-format, the value serves as the address and after the immediate data is provided to the processor, the index is added to the value to produce a new value in the data table pointer for a next immediate instruction,

if the format indicator comprises a pre-format, the index is added to the value to produce the address to the immediate data and the address is incremented by 1 after the immediate data is provided to the processor to produce a new value in the data table pointer for the next immediate instruction,

the format indicator comprises a binary bit having a logic 1 and logic 0 value, the logic 1 indicating one of pre-format or post-format and the logic 0 indicating other of pre-format or post-format,

the data table addressing unit further comprising,

a first adder comprising a first input coupled to the instruction register for receiving the index and a second input coupled to an output of the data table pointer for receiving the value contained therein,

a second adder comprising a first input coupled to the instruction register for receiving the format indicator, a second input coupled to an output of the first adder, and an output coupled to the data table pointer, and

a multiplexor comprising a first input coupled to an output of the data table pointer, a second input coupled to the output of the first adder, and a select input coupled to the instruction register for receiving the format indicator to select an multiplexor output from the first and second multiplexor inputs.

Claims 2-13 (cancelled)

14. (currently amended) The processor of claim 1[[3]] wherein the data table addressing unit comprises an incrementor for incrementing, ~~the incrementor increments~~ the address after the immediate data is provided to produce a new address for a new immediate instruction.

Claims 15-25 (cancelled)

26. (currently amended) The processor of claim 1 or 14 wherein the flow analysis comprises a static flow analysis, the static flow analysis to identifies immediate instructions within a program.

27. (original) The processor of claim 26 wherein an immediate instruction comprises addressing information to enable the processor to retrieve a corresponding immediate data to the immediate instruction.

28. (original) The processor of claim 27 wherein the addressing information comprises absolute addressing information.

29. (original) The processor of claim 27 wherein the addressing information comprises relative addressing information.

Claims 30-74. (cancelled)

75. (previously presented) A processor comprising:

a data table for storing immediate data of immediate instructions;

a program counter for storing an instruction address of an instruction, wherein the processor fetches the instruction from the instruction address in the program counter during program execution; and

an instruction decoder for decoding the instruction fetched by the processor, wherein immediate data from the data table is provided to the processor if the instruction is an immediate instruction;

an instruction register coupled to the instruction decoder, the instruction register stores the instruction fetched by the processor during program execution and passes the instruction to the instruction decoder for decoding;

a data table addressing unit comprising a data table pointer containing a value, the data table is coupled to the data table and instruction register, the instruction register passing relative addressing information contained in the instruction to the data table addressing unit when the decoder decodes the immediate instruction, the relative addressing information, which comprises an index and a format indicator, is used to provide an address of the immediate data in the data table, wherein the format indicator comprises a binary bit having a logic 1 and logic 0 value, the logic 1 indicating one of a pre-format or a post-format and the logic 0 indicating other of the pre-format or post-format;

if the format indicator indicates the post-format, the value serves as the address and after the immediate data is provided to the processor, the index is added to the value to produce a new value in the data table pointer for a next immediate instruction and if the format indicator indicates the pre-format, the index is added to the value to produce the address to the immediate data and the address is incremented by 1 after the immediate data is provided to the processor to produce a new value in the data table pointer for the next immediate instruction; and

wherein the addressing unit comprises

a first adder comprising a first input coupled to the instruction register for receiving the index and a second input coupled to an output of the data table pointer for receiving the value contained therein,

a second adder comprising a first input coupled to the instruction register for receiving the format indicator, a second input coupled to an output of the first adder, and an output coupled to the data table pointer, and

a multiplexor comprising a first input coupled to an output of the data table pointer, a second input coupled to the output of the first adder, and a select input coupled to the instruction register for receiving the format indicator to select an multiplexor output from the first and second multiplexor inputs.

76. (previously presented) A processor comprising:

a data table for storing immediate data of immediate instructions;

a program counter for storing an instruction address of an instruction, wherein the processor fetches the instruction from the instruction address in the program counter during program execution; and

an instruction decoder for decoding the instruction fetched by the processor, wherein immediate data from the data table is provided to the processor if the instruction is an immediate instruction;

an instruction register coupled to the instruction decoder, the instruction register stores the instruction fetched by the processor during program execution and passes the instruction to the instruction decoder for decoding;

a data table addressing unit comprising a data table pointer having a value, the data table addressing unit receives relative addressing information for decoded immediate instructions, the relative addressing information, which comprises an index and a format indicator, is used to provide an address of the immediate data in the data table;

if the format indicator indicates a post-format, the value serves as the address and after the immediate data is provided to the processor, the index is added to the value to produce a new value in the data table pointer for a next immediate instruction and if the format indicator indicates a pre-format, the index is added to the value to produce the address to the immediate data and the address is incremented by 1 after the immediate data is provided to the processor to produce a new value in the data table pointer for the next immediate instruction; and

wherein the addressing unit comprises

a first adder comprising a first input coupled to the instruction register for receiving the offset and a second input coupled to an output of the data table pointer for receiving the value contained therein,

a second adder comprising a first input coupled to the instruction register for receiving the format indicator, a second input coupled to an output of the first adder, and an output coupled to the data table pointer, and

a multiplexor comprising a first input coupled to an output of the data table pointer, a second input coupled to the output of the first adder, and a select input coupled to the instruction register for receiving the format indicator to select an multiplexor output from the first and second multiplexor inputs.